Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (canceled)

Claim 21 (new): An integrated circuit comprising:

a first processor unit to receive a first clock to control performance of the first processor unit;

a first buffer coupled to an output of the first processor unit, the first buffer clocked by a master clock;

a second processor unit to receive a second clock to control performance of the second processor unit; and

at least one clock controller to generate the first clock and the second clock, and to vary a frequency of the first clock and the second clock.

Claim 22 (new): The integrated circuit of claim 21, further comprising a memory coupled to the first processor unit and the second processor unit.

Claim 23 (new): The integrated circuit of claim 21, further comprising a wireless transceiver coupled to the first processor unit and the second processor unit.

Claim 24 (new): The integrated circuit of claim 21, wherein the first processor unit and the second processor unit comprise a reconfigurable processor core.

Claim 25 (new): The integrated circuit of claim 21, wherein the first buffer to provide a feedback signal to the at least one clock controller, the at least one clock controller to vary the first clock based on the feedback signal.

Claim 26 (new): The integrated circuit of claim 21, wherein the first clock is different than the master clock.

Claim 27 (new): The integrated circuit of claim 21, wherein the first processor unit comprises a reduced instruction set computer (RISC) processor.

Claim 28 (new): The integrated circuit of claim 21, wherein the first processor unit comprises a digital signal processor (DSP).

Claim 29 (new): The integrated circuit of claim 21, wherein the frequency is varied to optimize speed and processing power for a task.

Claim 30 (new): A system comprising:

a first processor to receive a first clock signal to control performance of the first processor;

a first buffer coupled to an output of the first processor; and

a first controller to generate the first clock signal from a master clock, the first controller to receive a first feedback signal from the first buffer and to control the first clock signal based on the first feedback signal to optimize processing power of the first processor.

Claim 31 (new): The system of claim 30, further comprising a second processor coupled to an output of the first buffer to receive a second clock signal to control performance of the second processor.

Claim 32 (new): The system of claim 30, wherein the first controller to provide a write signal to the first buffer based on the first feedback signal.

Claim 33 (new): The system of claim 30, wherein the first controller to lower a frequency of the first clock signal if the first feedback signal is above a threshold.

Claim 34 (new): The system of claim 30, wherein the system comprises a wireless device.

Claim 35 (new): The system of claim 34, further comprising an input sensor coupled to the first processor to receive visual information.

Claim 36 (new): A method comprising:

clocking a first processor of an integrated circuit with a first clock;

clocking a second processor of the integrated circuit with a second clock;

clocking a buffer coupled between the first processor and the second processor with a master clock; and

controlling a frequency of the first clock and the second clock to control performance of the first processor and the second processor.

Claim 37 (new): The method of claim 36, further comprising generating the first clock and the second clock from the master clock.

Claim 38 (new): The method of claim 36, further comprising generating the first clock and the second clock using a controller on a single substrate with the first processor and the second processor.

Claim 39 (new): The method of claim 38, further comprising generating a clock to control a wireless transceiver on the single substrate using the controller.